REMARKS/ARGUMENTS

Claims 1-15 were pending in the Application. By this Amendment, Claims 1 and 7 are being amended, Claims 13-15 are being cancelled, and new Claims 16-20 are being added, to advance the prosecution of the Application. No new matter is involved.

In Paragraph 2 which begins on page 2 of the Office Action, claims 1-12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art (APA) in view of published U.S. Application No. 2003/0058002 of Horiguchi. In Paragraph 3 which begins on page 4 of the Office Action, claims 13 and 14 are rejected under 35 U.S.C. § 103(a) as being unpatentable over APA, Horiguchi '002 and further in view of U.S. Patent 6,366,321 of Yonemoto, and in Paragraph 4 which begins on page 5 of the Office Action, claim 15 is rejected under 35 U.S.C. § 103(a) as being unpatentable over APA, Horiguchi '002 and further in view of published U.S. Application No. 2002/0000950 of Tonosaki et al. However, claims 13-15 are being cancelled herein, thereby obviating such rejections. The rejection of claims 1-12 as unpatentable over APA in view of Horiguchi '002 is respectfully traversed. Also, new claims 16-20 are submitted to clearly distinguish patentably over the prior art, as discussed hereafter.

In rejecting claims 1-12 as unpatentable over the combination of APA and Horiguchi '002, the Office Action states that APA teaches everything being claimed, in claim 1 for example, except for a control transistor connected between the amplification transistor and a second power source, wherein the control transistor cuts off a current flowing from the second power source to the amplification transistor according to a control signal. For this, Horiguchi is relied on. Horiguchi is said to teach a transistor to be used as a control transistor connected between a power source and a transistor such that when the gate voltage is brought to a low

level the current is cut off in order for the circuit to work in a lower power consumption mode.

In rejecting claims 13 and 14 on the combination of APA, Horiguchi '002 and Yonemoto '321, Yonemoto is relied on for its teaching that at the end of a read-out period, an imaging is performed and the drain current is extremely reduced in order to reduce the power consumption. In rejecting claim 15 on the combination of APA, Horiguchi '002 and Tonosaki '950, Tonosaki is relied on for a teaching that when the two-dimensional image is displayed in third or fourth modes, the consumed current at the time of use is reduced in order to reduce the power consumption.

Applicant has carefully reviewed the cited references and does not find them relevant to the present invention as claimed.

With respect to Horiguchi '002, while this reference describes a logical circuit capable of controlling the current, the reference fails to refer to application of a charge transfer device to a source follower circuit. Furthermore, Horiguchi '002 does not describe an output control circuit for controlling a source follower circuit according to the state of reading a pixel signal by the charge transfer device, an image capturing state, and image quality.

With respect to Yonemoto '321, this reference has an amplifying circuit which is an output circuit 16 (described at lines 36-43 of column 9). Such reference neither discloses nor suggests a specific structure of the output circuit 16 or reduction of a current flowing through the output circuit during a period with no video signal being read. Moreover, the description at line 66 of column 12 through line 3 of column 13 of the reference relates to signal reading from a pixel MOS transistor 1 to a load capacitor element 14, but not to the output circuit 16 serving as an amplifying circuit.

With respect to Tonosaki '950, this reference describes, in Paragraph [0013] thereof, that "when a two-dimensional image is displayed in the third mode or fourth mode, consumed current at the time of use is reduced by employing either of the two signal processing means". The third or fourth mode refers to, as described in Paragraph [0063], a mode of a system capable of displaying two video signals in two display devices, in which one video signal is processed and displayed in two display devices. That is, as the number of video signals to be processed is one, only one of the two signal processing means is used to process a signal. Thus, the third or fourth mode in Tonosaki does not concern quality of the video signal, but merely concerns a manner of displaying, specifically, either one of two video signals selectively processed and displayed in two display devices.

As amended, claim 1 is submitted to clearly distinguish patentably over the references. Claim 1 defines a charge transfer device having a source follower amplification circuit which comprises an amplification transistor, a load transistor and a control transistor. As amended, the circuit of claim 1 also includes "an output control circuit, connected to a gate of the control transistor, for outputting the control signal for reducing a current flowing from the second power source to the amplification transistor during a period in which a pixel signal is not read". As described above, none of the cited references, taken alone or in combination, show or suggest such features in accordance with the invention.

Claims 2-6 depend, directly or indirectly, from and contain all of the limitations of claim 1, so as to also distinguish patentably over the prior art.

As amended, claim 7 defines a charge transfer device having a source follower amplification circuit which comprises means for receiving at a gate, a voltage signal from an output section and outputting, from a source, an output signal corresponding to a change in the voltage signal. The circuit further includes means

for causing a constant current to flow from the means for receiving and outputting, to a side of a first power source connected between the means for receiving and outputting the first power source. The circuit still further includes means for controlling a current flowing from a second power source of the means for receiving and outputting according to a control signal connected between the means for receiving and outputting and the second power source. As amended herein, the circuit of claim 7 also includes "output control means, connected to the means for controlling a current, for outputting the control signal for reducing a current flowing from the second power source to the means for receiving and outputting during a period in which a pixel signal is not read". Thus, claim 7 as amended is also submitted to clearly distinguish patentably over the cited references.

Claims 8-12 depend, directly or indirectly, from and contain all of the limitations of claim 7, so that such claims are also submitted to clearly distinguish patentably over the art.

New claims 16 and 17 depend from and further define claim 7 in terms of "wherein the output control means, outputs the control signal for reducing a current flowing from the second power source to the means for receiving and outputting". In the case of claim 16, this occurs "while imaging is performed", while in the case of claim 17, this occurs "according to image quality".

New claim 18 depends from and further defines claim 1 in terms of "wherein the period in which a pixel signal is not read includes at least one of a horizontal blanking period and a vertical blanking period".

In addition to depending from and containing all of the limitations of either claim 1 or claim 7, new claims 16-18 define such claims in terms of additional limitations which are neither shown nor suggested by any of the cited references.

Therefore, new claims 16-18 are submitted to clearly distinguish patentably over the prior art.

New claims 19 and 20 define a charge transfer device having a source follower amplification circuit which comprises an amplification transistor, a load transistor, a control transistor and an output control circuit "connected to the gate of the control transistor, for outputting the control signal for reducing a current flowing from the second power source to the amplification transistor". In the case of claim 19, this is defined as occurring "while imaging is performed", while in the case of claim 20, it is defined as occurring "according to image quality".

Therefore, new claims 19 and 20 are submitted to clearly distinguish patentably over the art.

In conclusion, claims 1-12 and 16-20 are submitted to clearly distinguish patentably over the art for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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